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Title:

**CMOS IMAGER AND METHOD OF FORMATION**

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## **CMOS IMAGER AND METHOD OF FORMATION**

### **FIELD OF THE INVENTION**

[0001] The present invention relates to the field of semiconductor devices and, in particular, to high quantum efficiency CMOS image sensors.

### **BACKGROUND OF THE INVENTION**

[0002] CMOS imagers have been increasingly used as low cost imaging devices. A CMOS imager circuit includes a focal plane array of pixel cells, each one of the cells including either a photodiode, a photogate or a photoconductor overlying a doped region of a substrate for accumulating photo-generated charge in the underlying portion of the substrate. A readout circuit is connected to each pixel cell and includes a charge transfer section formed on the substrate adjacent the photodiode for transferring electrons to a sensing node, typically a floating diffusion node, connected to the gate of a source follower output transistor. The imager may include at least one transistor for transferring charge from the charge accumulation region of the substrate to the floating diffusion node and also has a transistor for resetting the diffusion node to a predetermined charge level prior to charge transfer.

[0003] In a conventional CMOS imager, the active elements of a pixel cell perform the necessary functions of: (1) photon to charge conversion; (2) accumulation of image charge; (3) transfer of charge to the floating diffusion node accompanied by charge amplification; (4) resetting the floating diffusion node to a known state before the transfer of charge to it; (5) selection of a pixel for readout; and (6) output and amplification of a signal representing pixel charge. The charge at the floating diffusion node is converted to a pixel output voltage by the source follower output transistor. The photosensitive element of a CMOS imager pixel is typically either a depleted p-n junction photodiode or a field induced depletion region beneath a photogate.

[0004] CMOS imaging devices of the type discussed above are generally known and discussed in, for example, Nixon et al., "256.times.256 CMOS Active Pixel Sensor Camera-on-a-Chip," IEEE Journal of Solid-State Circuits, Vol. 31(12), pp. 2046-2050 (1996); and Mendis et al., "CMOS Active Pixel Image Sensors," IEEE Transactions on Electron Devices, Vol. 41(3), pp. 452-453 (1994), the disclosures of which are incorporated by reference herein.

[0005] A schematic top view of a semiconductor wafer fragment of an exemplary CMOS sensor pixel four-transistor (4T) cell 10 is illustrated in Figure 1. As it will be described below, the CMOS sensor pixel cell 10 includes a photo-generated charge accumulating area 21 in an underlying portion of the substrate. This area 21 is formed as a pinned diode 11 (Figure 2). The pinned photodiode is termed "pinned" because the potential in the photodiode is pinned to a constant value when the photodiode is fully depleted. It should be understood, however, that the CMOS sensor pixel cell 10 may include a photogate, a photoconductor or other image to charge converting

device, in lieu of a pinned photodiode, as the initial accumulating area 21 for photo-generated charge.

[0006] The CMOS image sensor 10 of Figure 1 has a transfer gate 30 for transferring photoelectric charges generated in the charge accumulating region 21 to a floating diffusion region (sensing node) 25. The floating diffusion region 25 is further connected to a gate 50 of a source follower transistor. The source follower transistor provides an output signal to a row select access transistor having gate 60 for selectively gating the output signal to terminal 32. A reset transistor having gate 40 resets the floating diffusion region 25 to a specified charge level before each charge transfer from the charge accumulating region 21.

[0007] A cross-sectional view of the exemplary CMOS image sensor 10 of Figure 1 taken along line 2-2' is illustrated in Figure 2. The charge accumulating region 21 is formed as a pinned photodiode 11 which has a photosensitive or p-n-p junction region formed by a p-type layer 24, an n-type region 26 and the p-type substrate 20. The pinned photodiode 11 includes two p-type regions 20, 24 so that the n-type photodiode region 26 is fully depleted at a pinning voltage. Impurity doped source/drain regions 22 (Figure 1), preferably having n-type conductivity, are provided on either side of the transistor gates 40, 50, 60. The floating diffusion region 25 adjacent the transfer gate 30 is also preferable n-type.

[0008] Figure 2 also illustrates trench isolation regions 15 formed in the active layer 20 adjacent the charge accumulating region 21. The trench isolation regions 15 are typically formed using a conventional STI process or by using a Local Oxidation of Silicon (LOCOS) process. A translucent or transparent insulating layer 55

formed over the CMOS image sensor 10 is also illustrated in Figure 2. Conventional processing methods are used to form, for example, contacts 32 (Figure 1) in the insulating layer 55 to provide an electrical connection to the source/drain regions 22, the floating diffusion region 25, and other wiring to connect to gates and other connections in the CMOS image sensor 10.

[0009] Generally, in CMOS image sensors such as the CMOS image sensor cell 10 of Figures 1-2, incident light causes electrons to collect in region 26. A maximum output signal, which is produced by the source follower transistor having gate 50, is proportional to the number of electrons to be extracted from the region 26. The maximum output signal increases with increased electron capacitance or acceptability of the region 26 to acquire electrons. The electron capacity of pinned photodiodes typically depends on the doping level of the image sensor and the dopants implanted into the active layer.

[0010] Minimizing dark current in the photodiode is important in CMOS image sensor fabrication. Dark current is generally attributed to leakage in the charge collection region 21 of the pinned photodiode 11, which is strongly dependent on the doping implantation conditions of the CMOS image sensor. In addition, defects and trap sites inside or near the photodiode depletion region strongly influence the magnitude of dark current generated. In sum, dark current is a result of current generated from trap sites inside or near the photodiode depletion region; band-to-band tunneling induced carrier generation as a result of high fields in the depletion region; junction leakage coming from the lateral sidewall of the photodiode; and leakage from isolation corners, for example, stress induced and trap assisted tunneling.

[0011] CMOS imagers also typically suffer from poor signal to noise ratios and poor dynamic range as a result of the inability to fully collect and store the electric charge collected in the region 26. Since the size of the pixel electrical signal is very small due to the collection of photons in the photo array, the signal to noise ratio and dynamic range of the pixel should be as high as possible.

[0012] There is needed, therefore, an improved active pixel photosensor for use in a CMOS imager that exhibits reduced dark current and increased photodiode capacitance, while also having low pixel-to-pixel cross-talk. A method of fabricating an active pixel photosensor exhibiting these improvements is also needed.

### **BRIEF SUMMARY OF THE INVENTION**

[0013] In one aspect, the invention provides a deep implanted region of a first conductivity type located below a transistor array of a pixel sensor cell and laterally adjacent a doped region of a second conductivity type of a photodiode of the pixel sensor cell. The deep implanted region reduces surface leakage and dark current and increases the capacitance of the photodiode by acting as a reflective barrier to electrons generated by light in the doped region of the second conductivity type of the photodiode. The deep implanted region also provides optimal transfer of charges from the charge collection region to a floating diffusion region adjacent the gate of the transfer transistor.

[0014] In another aspect, the invention provides a method of forming a deep implanted region below a transistor array of a pixel

sensor cell and laterally adjacent a charge collection region of a photodiode of the pixel sensor cell. The deep implanted region is formed by conducting at least one deep implant for implanting desired dopants below the transistor array and subsequent to the patterning of the transistor gate structures of the pixel sensor cell.

[0015] These and other features and advantages of the invention will be more apparent from the following detailed description that is provided in connection with the accompanying drawings and illustrated exemplary embodiments of the invention.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0016] Figure 1 is a top plan view of an exemplary CMOS image sensor pixel.

[0017] Figure 2 is a schematic cross-sectional view of the CMOS image sensor of Figure 1 taken along line 2-2'.

[0018] Figure 3 is a schematic cross-sectional view of a CMOS image sensor pixel fabricated in accordance with the present invention and at an initial stage of processing.

[0019] Figure 4 is a schematic cross-sectional view of a CMOS image sensor fragment of Figure 3 at a stage of processing subsequent to that shown in Figure 3.

[0020] Figure 5 is a schematic cross-sectional view of a CMOS image sensor pixel of Figure 3 at a stage of processing subsequent to that shown in Figure 4.

[0021] Figure 6 is a schematic cross-sectional view of a CMOS image sensor pixel of Figure 3 at a stage of processing subsequent to that shown in Figure 5.

[0022] Figure 7 illustrates a schematic diagram of a computer processor system incorporating a CMOS image sensor fabricated according to the present invention.

### **DETAILED DESCRIPTION OF THE INVENTION**

[0023] In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention.

[0024] The terms “wafer” and “substrate” are to be understood as a semiconductor-based material including silicon, silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a “wafer” or “substrate” in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor structure or foundation. In addition, the semiconductor need not be silicon-based, but could be based on silicon-germanium, silicon-on-



insulator, silicon-on-sapphire, germanium, or gallium arsenide, among others.

[0025] The term “pixel” refers to a picture element unit cell containing a photosensor and transistors for converting electromagnetic radiation to an electrical signal. For purposes of illustration, a representative pixel is illustrated in the figures and description herein and, typically, fabrication of all pixels in an imager will proceed simultaneously in a similar fashion.

[0026] Referring now to the drawings, where like elements are designated by like reference numerals, Figures 3-6 illustrate exemplary embodiments of methods of forming a four-transistor (4T) pixel sensor cell 100 (Figure 6) having a deep implanted region or well 199 formed below a transistor array 101 and adjacent a charge collection region 126 of photodiode 188. As explained in detail below, the deep implanted region 199 is formed by implanting dopants of a first conductivity type below the transistor array 101 and in the bulk substrate 110. The deep implanted region 199 is adjacent a doped region 126 of a second conductivity type forming the charge collection region of the photodiode 188 and acts as a reflective barrier to electrons generated by light in the doped region 126 of the second conductivity type.

[0027] It should be noted that, although the invention will be described below in connection with use in a four-transistor (4T) pixel cell, the invention also has applicability to a three-transistor (3T) cell which differs from the 4T cell in the omission of a charge transfer transistor described below, as known in the art. In this case, the deep implant is still located adjacent the charge collection region of a photodiode.

[0028] Figure 3 illustrates a substrate 110 along a cross-sectional view of the structure of Figure 1 taken along line 3-3'. For exemplary purposes, the substrate 110 is a silicon substrate. However, as noted above, the invention has equal application to other semiconductor substrates. Figure 3 also illustrates a multi-layered transfer and reset gate stacks 130 and 140, respectively, formed over the silicon substrate 110 and as part of transistor array 101. The transfer and reset gate stacks 130 comprise a first gate oxide layer 131 of grown or deposited silicon oxide on the silicon substrate 110, a conductive layer 132 of doped polysilicon or other suitable conductor material, and a second insulating layer 133, which may be formed of, for example, silicon oxide (silicon dioxide), nitride (silicon nitride), oxynitride (silicon oxynitride), ON (oxide-nitride), NO (nitride-oxide), or ONO (oxide-nitride-oxide). The first and second insulating layers 131, 133 and the conductive layer 132 may be formed by conventional deposition methods, for example, chemical vapor deposition (CVD) or plasma enhanced chemical vapor deposition (PECVD), among many others.

[0029] If desired, a silicide layer (not shown) may be also formed in the multi-layered gate stacks 130, 140 between the conductive layer 132 and the second insulating layer 133. Advantageously, the gate structures of all other transistors in the imager circuit design may have this additionally formed silicide layer. This silicide layer may be titanium silicide, tungsten silicide, cobalt silicide, molybdenum silicide, or tantalum silicide. The silicide layer could also be a barrier layer/refractory metal such as TiN/W or  $WN_x$ /W or it could be entirely formed of  $WN_x$ . Figure 3 also illustrates insulating sidewall spacers 134 formed on the sides of the transfer gate 130 and of the reset gate 140. The sidewall spacers 134 may be formed, for example,

of silicon dioxide, silicon nitride, silicon oxynitride, ON, NO, ONO or TEOS, among others.

[0030] Figure 3 also illustrates isolation regions 150 which are formed within the substrate 110 and are filled with a dielectric material, which may be an oxide material, for example a silicon oxide such as SiO or SiO<sub>2</sub>, oxynitride, a nitride material such as silicon nitride, silicon carbide, or other suitable dielectric materials. In a preferred embodiment, however, the isolation regions 150 are shallow trench isolation regions and the dielectric material is a high density plasma (HDP) oxide, a material which has a high ability to effectively fill narrow trenches. Thus, for simplicity, reference to the isolation regions 150 will be made in this application as to the shallow trench isolation regions 150. The shallow trench isolation regions 150 have a depth of about 1,000 to about 4,000 Angstroms, more preferably of about 2,000 Angstroms.

[0031] Although Figures 3-6 illustrate only a portion of the substrate 110 with only two shallow trench isolation regions 150, it must be understood that the present invention contemplates the simultaneous formation of more than two shallow trench isolation structures at various locations on the substrate 110 to isolate the pixels one from another and to isolate other structures as well.

[0032] In addition, if desired, a thin insulating layer (not shown) may be formed on the sidewalls and bottom of the shallow trench before the filling of the trench with the dielectric material which, as noted above, is preferably a high density plasma (HDP) oxide. The thin insulating layer may be formed of an oxide or of silicon nitride, for example, to aid in smoothing out the corners in the bottom of the

trench and to reduce the amount of stress in the dielectric material used to later fill in the trenches.

[0033] Referring now to Figure 4, a p-n-p photodiode 188 is formed by regions 124, 126 and 120 within the substrate 110. The p-type doped layer 120 is formed in the areas of the substrate 110 directly beneath the active area of the pixel cell by conducting a dopant implantation with a dopant of a first conductivity type, which for exemplary purposes is p-type. The p-type doped layer 120 may be formed subsequent to the formation of the shallow trench isolation (STI) 150 and of the gate stacks 130, 140. However, it must be understood that the p-type doped layer 120 may be also formed prior to the formation of the shallow trench isolation (STI) 150 and/or gate stacks 130, 140. The dopant concentration in the p-type doped layer 120 is within the range of about  $1 \times 10^{15}$  to about  $5 \times 10^{18}$  atoms per  $\text{cm}^3$ , and is preferably within the range of about  $1 \times 10^{16}$  to about  $5 \times 10^{17}$  atoms per  $\text{cm}^3$ .

[0034] The n-type region 126 (Figure 4) is formed by implanting dopants of a second conductivity type, which for exemplary purposes is n-type, in the area of the substrate directly beneath the active area of the pixel cell. The implanted n-doped region 126 forms a photosensitive charge storage region for collecting photogenerated electrons. Ion implantation may be conducted by placing the substrate 110 in an ion implanter, and implanting appropriate n-type dopant ions into the substrate 110 at an energy of 20 keV to 300 keV to form n-doped region 126. N-type dopants such as arsenic, antimony, or phosphorous may be employed. The dopant concentration in the n-doped region 126 (Figure 4) is within the range of about  $5 \times 10^{15}$  to about  $5 \times 10^{16}$  atoms per  $\text{cm}^3$ , and is preferably within the range of about  $1 \times 10^{16}$  to about  $5 \times 10^{16}$  atoms per  $\text{cm}^3$ .

[0035] The p-type pinned surface layer 124 is also formed by conducting a dopant implantation with a dopant of the first conductivity type, which for exemplary purposes is p-type, so that p-type ions are implanted into the area of the substrate over the implanted n-type region 126 and between the transfer gate 130 and shallow trench isolation region 150. The dopant concentration in the p-type pinned surface layer 124 is within the range of about  $1 \times 10^{17}$  to about  $5 \times 10^{18}$  atoms per  $\text{cm}^3$ , and is preferably within the range of about  $1 \times 10^{18}$  atoms per  $\text{cm}^3$ .

[0036] Subsequent to the formation of the p-n-p photodiode 188 and of the transfer and reset gates 130, 140, a photoresist layer 167 (Figure 5) is formed over the p-n-p photodiode 188 and the transfer and reset gates 130, 140, to a thickness of about 1,000 Angstroms to about 10,000 Angstroms. The photoresist layer 167 (Figure 5) is patterned with a mask (not shown) to obtain an opening 168 (Figure 5) which, on one side, partially extends over transfer gate 130 by an offset distance W, as illustrated in Figure 5 and, on the other side, is approximately coincident with the edge of the STI region 150 (the left most STI region in Figure 5).

[0037] The offset distance W (Figure 5) may be tailored according to the photodiode and transfer gate characteristics to achieve an optimal dopant gradient from the n-type charge collection region 126 of the photodiode 188 to n-type floating diffusion region 129. The offset distance W may be about 10% to about 90% the length L (Figure 5) of the transfer gate 130, more preferably of about 25% to about 75% the length L of the transfer gate 130. For example, a transfer gate having a length L of about 0.5 microns may require an offset distance W of about 50% the length of the transfer gate, that is, of about 0.25 microns. Similarly, a transfer gate having a length L of about 0.3

microns may require an offset distance  $W$  of about 25% the length of the transfer gate, that is, of about 0.13 microns.

[0038] Next, the structure of Figure 5 is subjected to a deep masked dopant implantation 169 (Figure 5) with a dopant of the first conductivity type, which for exemplary purposes is p-type. This way, p-type ions are implanted through the opening 168 (Figure 5) to form a p-type deep implanted region 199 located below the transistor array 101 and in contact with the n-type doped region 126, as illustrated in Figure 6. Although, the p-type deep implanted region 199 may be formed in contact with the n-type doped region 126, as shown in Figure 6, the invention is not limited to this embodiment. Accordingly, the present invention also contemplates the formation of a p-type deep implanted region adjacent and spaced from the n-type doped region 126, in accordance with the photodiode and transfer gate characteristics.

[0039] The deep dopant implantation 169 is conducted to implant p-type ions, such as boron, beryllium, indium or magnesium, into an area of the substrate 110 located right below the transistor array 101. The dopant implantation 169 may be conducted by placing the substrate 110 in an ion implanter and implanting appropriate p-type dopant ions through the opening 168 (Figure 5) into the substrate 110 at an energy of 50 keV to about 150 keV, more preferably of about 90 keV, to form the deep p-type implanted region or well 199. P-type dopants, such as boron, beryllium, indium or magnesium, may be employed for the first implant. The dopant concentration in the deep p-type implanted region 199 (Figure 6) is within the range of about  $1 \times 10^{16}$  to about  $1 \times 10^{17}$  atoms per  $\text{cm}^3$ , more preferably of about  $5 \times 10^{15}$  to about  $5 \times 10^{16}$  atoms per  $\text{cm}^3$ .

[0040] The photoresist layer 167 is then removed by conventional techniques, such as oxygen plasma for example, or by flooding the substrate 110 with UV radiation, to complete the formation of deep implanted region 199 (Figure 6) and the formation of the pixel sensor cell 100 (Figure 6).

[0041] The deep implanted region 199 of Figure 6 acts as a reflective barrier to electrons generated by light in the n-doped region 126 of the p-n-p photodiode 188. When light radiation in the form of photons strikes the n-doped photosite region 126, photo-energy is converted to electron-hole pairs. For the case of an n-doped photosite in a p-n-p photodiode, it is the electrons that are accumulated in the n-doped region 126. For the case of a p-doped photosite in an n-p-n photodiode, it is the holes that are accumulated in the n-doped region 126. Thus, in the exemplary embodiment described above having n-channel devices formed in the p-type well 120, electrons are accumulated in the n-doped region 126. The deep implanted region 199 located below the transistor array 101 acts to reduce carrier loss to the substrate 110 by forming a concentration gradient that modifies the band diagram and serves to reflect electrons back towards the n-doped photosite region 126, thereby reducing cross-talk between adjacent pixel sensor cells.

[0042] In addition to providing a reflective barrier to electrons generated by light in the charge collection region 126, the deep implanted region 199 creates a dopant gradient from the photodiode 188 to the floating diffusion region 129 (Figure 6). As known in the art, one figure of merit (FoM) of the transfer gate 130 is the efficiency of the gate 130 to transfer accumulated charge from the photodiode region 126 to the floating diffusion region 129. One way of increasing the transfer efficiency of the gate 130 is to physically apply a potential

gradient  $V_t$  from the photodiode region 126 to the floating diffusion region 129. The present invention provides another way of increasing the transfer efficiency of the gate 130, that is, by creating a dopant gradient conferred by the deep implanted region 199 (Figure 6) that optimizes the transfer of charge from the photodiode region 126 to the floating diffusion region 129.

[0043] The deep implanted region 199 also provides photodiode-to-photodiode isolation, for example, isolation of the photodiode 188 from an adjacent photodiode (not shown) located on the other side of the shallow trench isolation region 150.

[0044] Although Figures 3-6 illustrate deep implanted region 199 formed by conducting only one implant, the invention is not limited to this embodiment and contemplates the formation of a deep implanted region formed by conducting a plurality “i” of such deep implants. Preferably, the number “i” of implants and the dopant concentration of each implant may be tailored so that depth D (Figure 6) of the deep implanted region 199 is equal to or greater than the depth of the n-type doped region 126 of the photodiode 188. This way, one skilled in the art may tailor the dosage and implant energy of each of the “i” implants to form the deep implanted region 199 which acts as a barrier to fully reflect electrons back toward the n-doped photosite region 126 and provide complete isolation of the photodiode 188 from adjacent photodiodes. Preferably, the depth D of the p-type implanted region 199 of the substrate 110 may be of about 0.5 microns to about 7.0 microns, more preferably of about 1.0 microns to about 5.0 microns.

[0045] The remaining devices of the pixel sensor cell 100, including the source follower transistor and row select transistor shown in Figure 1 as associated with respective gates 50 and 60 and



source/drain regions on either sides of the gates 40, 50, 60, are also formed by well-known methods. Conventional processing steps may be also employed to form contacts and wiring to connect transistor gate and source and drain regions of pixel cell 100. For example, the entire surface may be covered with a passivation layer 155 (Figure 6) of, e.g., silicon dioxide, BSG, PSG, or BPSG, which is CMP planarized and etched to provide contact holes, which are then metallized to provide contacts to the reset gate, transfer gate and other pixel structures, as needed. Conventional multiple layers of conductors and insulators to other circuit structures may also be used to interconnect the internal structures of the pixel sensor cell and to connect the pixel cell structures to other circuitry associated with the pixel array.

[0046] A typical processor based system 600, which has a connected CMOS imager having pixels constructed according to the invention is illustrated in Figure 7. A processor based system is exemplary of a system having digital circuits which could include CMOS imagers. Without being limiting, such a system could include a computer system, camera system, scanner, machine vision, vehicle navigation, video phone, surveillance system, auto focus system, star tracker system, motion detection system, image stabilization system and data compression system for high-definition television, all of which can utilize the present invention.

[0047] A processor based system, such as a computer system, for example generally comprises a central processing unit (CPU) 644, for example, a microprocessor, that communicates with an input/output (I/O) device 646 over a bus 652. The CMOS imager 642 communicates with the system over bus 652. The computer system 600 also includes random access memory (RAM) 648, and may include peripheral devices such as a floppy disk drive 654, and a compact disk

(CD) ROM drive 656 or a flash memory card 657 which also communicate with CPU 644 over the bus 652. It may also be desirable to integrate the processor 654, CMOS image sensor 642 and memory 648 on a single IC chip.

[0048] Although the above embodiments have been described with reference to the formation of a p-n-p photodiode, such as the p-n-p photodiode 188 (Figures 3-6) having an n-type charge collection region formed adjacent a deep implanted region 199 formed by implantation below a transistor array, it must be understood that the invention is not limited to this embodiment. Accordingly, the invention has equal applicability to n-p-n photodiodes comprising an p-type charge collection region formed adjacent a p-type deep implanted region formed below a transistor array. Of course, the dopant and conductivity type of all structures will change accordingly, with the transfer gate corresponding to a PMOS transistor. The invention has further applicability to p-n or n-p photodiodes, that is, photodiodes that do not include a “pinned” or “surface” layer.

[0049] In addition, although the invention has been described above with reference to a transfer gate of a transfer transistor connection for use in a four-transistor (4T) pixel cell, the invention also has applicability to a three-transistor (3T) cell which differs from the 4T cell in the omission of a charge transfer gate 130, the formation of which was described above. In this case, the deep implanted region 199 is still formed to be laterally adjacent a charge collection region 126.

[0050] The above description and drawings are only to be considered illustrative of exemplary embodiments, which achieve the features and advantages of the invention. Modification and

substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the invention.

Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.